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DOCUMENT-IDENTIFIER: US 6323121 B1
TITLE: Fully dry post-via-etch cleaning method for a damascene process

Abstract Text (1):
A method is described for cleaning freshly etched dual damascene via openings and preparing them for copper fill without damage or contamination of exposed organic or other porous low-k insulative layers. The method is entirely dry and does not expose the porous materials to contamination from moisture or solvents. The method is effective for removing all traces of residual polymer deposits from an in-process substrate wafers after via or damascene trench etching. The method employs an in-situ three-step treatment comprising a first step of exposing the electrically biased substrate wafer to a O.sub.2 /N.sub.2 ashing plasma to remove photoresist and polymers, a second step immediately following the first step of remove silicon nitride etch stop layers, and a final step of treating the wafer with H.sub.2 /N.sub.2 to remove copper polymer deposits formed during nitride removal. The H.sub.2 /N.sub.2 plasma is capable of removing the difficult polymer residues which are otherwise only removable by wet stripping procedures. The H.sub.2 /N.sub.2 plasma is not harmful to exposed porous low-k dielectric layers as well as copper metallurgy.

Brief Summary Text (8):
In order to further improve circuit performance, low dielectric constant (low-k) insulative materials have been incorporated into the dielectric layers of modern integrated circuits. These materials provide a lower capacitance than conventional silicon oxide and consequently, an increase in circuit speed. Lou, et.al., U.S. Pat. No. 5,916,823 shows a method for forming a dual damascene structure using a low-k SOG (spin-on-glass). SOGs are alcohol soluble siloxanes or silicates which are spin deposited and baked to drive off solvents resulting in a relatively porous silicon oxide structure. Other porous silica structures such as xerogels have been developed, notably by Texas Instruments Inc. and incorporated into dual damascene processes to obtain insulative layers with dielectric constants as low as 1.3. This is to be compared with a dielectric constant of about 4 for conventional silicon oxide. Other organic and quasi-organic materials such as polysilsesquioxanes and polyarylene ethers have been added to the growing family of low-k and ultra low-k insulative materials. The materials are deposited either by spin-on deposition or by CVD (Chemical vapor deposition).

Brief Summary Text (9):
Although these materials offer welcome improvement in circuit performance, they also pose problems in processing. Because they are very porous, they are not only prone to absorb and retain contaminants, in particular moisture and solvents, but they also react to a large extent with wet processing chemistries such as those used for cleaning and removing residues left after plasma etching and photoresist stripping. In Dai, solvents are removed by baking and a cap oxide liner is deposited on the walls of the etched damascene openings to seal the SOG surfaces against contamination. Whereas Dai uses an oxygen ashing process followed by wet stripping with H.sub.2 SO.sub.4, H.sub.2 O.sub.2, and NH.sub.4 OH to remove photoresist and other residues after the via etch such treatment would be damaging to OSOGs (organic spin-on-glasses) and some other low-k insulative materials including those deposited by CVD.

Brief Summary Text (10):

Jeng, U.S. Pat. No. 5,453,157 teaches an anisotropic, low temperature (-40.degree. C. to 20.degree. C.), oxygen plasma ashing process which does not harm the exposed edges of low-k OSOG underlayers. The ashing plasma is made directional with respect to the wafer by biasing the wafer to attract the positively charged oxygen species. In addition, the wafer must be cooled during the ashing, for example by liquid nitrogen.

Brief Summary Text (11):
Fujimura, et.al., U.S. Pat. No. 5,773,201 teaches another photoresist ashing process wherein ashing takes place in a chamber located downstream of an oxygen plasma source. It is shown that hydrogen or water vapor, added to the oxygen plasma, lowers the activation energy of the ashing process. However, hydrogen addition, even in small amounts, creates an explosion hazard. The addition of nitrogen or water vapor to the oxygen plasma increases the ashing rate by increasing the concentration of oxygen atoms in the plasma.

Brief Summary Text (14):
In addition, wet etchant chemistries also cause damage to exposed copper surfaces which are exposed in certain copper damascene via processes wherein the wet etch clean is used after copper is exposed at the base of the via openings. These residues may no longer be removed by conventional wet etching because of the interaction of the wet etchants with exposed low-k dielectric layers. Oftentimes, for reasons of design or process integration, the edges of low-k dielectric layers, cannot be sealed in the manner of Lou, '823, to prevent exposure of the edges to a wet cleaning step.

Brief Summary Text (15):
It is therefore desirable to have a totally dry process which provides a highly but not totally anisotropic cleaning action without damaging or contaminating exposed lateral edges of low-k organic and doped silicaceous structural layers. In addition, the process should provide means to protect metal exposed at the base of the via opening. The method taught by this invention is such a process.

Brief Summary Text (17):
Accordingly, it is an object of this invention to provide a totally dry method for removing photoresist and sidewall polymer from a freshly etched damascene via opening, removing an etch stop at the base of the via opening, and cleaning out copper polymers left by the etch stop removal process, without damaging or contaminating exposed low-k dielectric layers.

Brief Summary Text (20):
These objects are accomplished by an in-situ three-step plasma treatment comprising a first step of exposing the substrate wafer, after via etching, to a O.sub.2 /N.sub.2 ashing plasma, a second step immediately following the first step in the same chamber, and without breaking vacuum, of removing the etch stop layer and a third step of treating the wafer with a H.sub.2 /N.sub.2 plasma to remove copper polymer residues which remain after the etch stop removal. The H.sub.2 /N.sub.2 plasma is capable of removing difficult polymer residues which are otherwise only removable by wet stripping procedures. The H.sub.2 /N.sub.2 plasma is not harmful to the exposed porous low-k dielectric layers. Because the process is completely dry, the absorption of moisture or solvents by porous low-k layers is avoided.

Drawing Description Text (2):
FIG. 1A through FIG. 1F are cross sections of a silicon wafer illustrating a sequence of processing steps for forming a via and a layer of copper metallization in the presence of low-k insulative layers by a dual damascene process according to an embodiment of this invention.

Detailed Description Text (5):
A low-k dielectric layer 18 is next formed over the wafer 10 by a CVD method, preferably by HDP (high density plasma) CVD or by PECVD to a thickness of between about 0.5 and 0.7 microns. CVD deposited low-k materials which may be used include fluorinated silicate glasses (FSG), sometimes called fluorinated oxide, Organosilicate glasses (OSG), for example Black Diamond.TM., from Applied Materials Corporation of Santa Clara Calif., films formed from a methylated silane, and the more recently investigated FLAC (fluorinated amorphous carbon) films.

Detailed Description Text (6):
A second layer of silicon nitride 20 is next deposited on the low-k layer 18 by PECVD. Again, another deposition means may alternately be used to deposit this layer, however, PECVD is preferred because of the beneficial low deposition temperature. The silicon nitride layer 20 is deposited to a thickness of between about 300 and 500 Angstroms. A second low-k dielectric layer 22 is deposited on the silicon nitride layer 20 using the same procedures as are employed in the formation of the first low-k dielectric layer 18. The second low-k layer 22 is between about 0.5 and 1.0 microns thick and may be formed of the same low-k material as the first low-k layer 18 or of one of the alternate low-k material cited above for the layer 18.

Detailed Description Text (7):
A layer of silicon oxynitride 24 is deposited on the second low-k dielectric layer 22. The silicon oxynitride layer 24 is deposited by PECVD using SiH.sub.4 and N.sub.2 O in a He carrier gas and is between about 200 and 600 Angstroms thick. Process parameters for PECVD deposition of silicon oxynitride are well known to those skilled in the art.

Detailed Description Text (9):
The via opening 8 is etched in a single operation, by reactive ion etching sequentially, through the silicon oxynitride layer 24, the low-k dielectric layer 22, the silicon nitride layer 20 and the low-k dielectric layer 18, stopping on the silicon nitride layer 16. Reactant gas mixtures and etching parameters are adjusted for each layer to achieve a high etch rate for each layer as it is reached. An endpoint sensor, such as an optical emission spectrometer, provides continuous monitoring of the etching process and indicates when etchant gases are to be changed to accommodate either a nitride layer or an insulative layer. The nitride layers are etched with a gas mixture containing a fluorocarbon such as CF.sub.4 and oxygen, while the insulative layers are etched with fluorocarbons alone, for example CHF.sub.3 or C.sub.4 F.sub.8. Etchant gas mixtures and plasma parameters for etching the various layers are well known to those in the art and can be experimentally optimized for each application. Stopping on the silicon nitride layer 16 is easily achieved by utilizing etching parameters which provide a high insulative layer-to-silicon nitride selectivity.

Detailed Description Text (14):
Although the silicon oxynitride BARC 24 still remains over the low-k layer 22, the spun-on BARC 28 has the added purpose of protecting the nitride etch stop layer 16 at the bottom of the trench 8. When the BARC 28 is spun onto the wafer, a portion 28A is captured and retained in the opening 8 during the spin-on process. The portion 28A is much thicker than the BARC 28 over the planar regions and subsequently, enough remains to protect the silicon nitride layer 16 at the base of the opening 8 during subsequent etching of the wider or trench portion of the dual damascene structure.

Detailed Description Text (15):
A photoresist layer 30 is next patterned on the wafer 10 to define the wider or trench portion 9 of the dual damascene structure. Referring to FIG. 1D, the BARC 28, the silicon oxynitride layer 24, and the low-k organic layer 22 are etched to the silicon nitride etch stop layer 20, forming the trench 9. The etching process is accomplished in the same etching chamber that was previously used to form the via opening 8. The wafer 10 is next transferred to the ashing chamber and the residual photoresist layer 30, the thin BARC 28 under the photoresist, as well as the BARC portion 28A in the via opening are removed by ashing in a O.sub.2 /N.sub.2 plasma. The O.sub.2 is flowed at a rate of between about 20 and 80 SCCM and N.sub.2 at a flow rate of between about 20 and 80 SCCM. The chamber pumping speed is throttled to maintain a chamber pressure of between about 50 and 100 milliTorr. During ashing a bias power of between about 500 and 700 Watts is applied to the substrate to provide plasma directionality and the temperature of the wafer is maintained at between about 40 and 60.degree. C. by controlling the temperature of a pedestal in the ashing tool upon which the wafer rests.

Detailed Description Text (16):
FIG. 1E shows the structure after the O.sub.2 /N.sub.2 ashing treatment. In order to prepare the dual damascene opening 8,9 for copper deposition, the silicon nitride layer 16 must be removed at the base of the via opening 8. This is accomplished directly after the O.sub.2 /N.sub.2 ashing treatment, and in the same chamber without breaking vacuum, by plasma etching in a plasma containing fluorocarbons

and oxygen. Fluorocarbon/oxygen etchant gas mixtures and plasma parameters for etching silicon nitride are well known to those in the art and can be experimentally optimized to etch the nitride with minimum over-etch. A bias power of between about 500 and 700 Watts is applied to the substrate to provide plasma directionality. The silicon nitride layer 16 in the via opening 8 as well as the exposed portions of the silicon nitride layer 20 and the silicon oxynitride BARC 24 are removed with negligible attack of the low-k dielectric layers. The silicon oxynitride 24 and the exposed silicon nitride 20 are concurrently removed along with the exposed etch stop nitride 16.

Detailed Description Text (20):
While the embodiment of the invention utilizes a CVD deposited low-k dielectric layers for each of the two insulative sections of the dual damascene structure, the procedures taught by this invention for forming and cleaning a dual damascene structure can be applied equally well using other low-k insulative materials such as the various porous low-k silicaceous dielectric materials deposited either by CVD or by spin-on techniques, such as aerogels, silica gels, or polysilsesquioxanes. In addition the all dry via forming process taught by this invention may be applied when conventional dielectrics such as silicon oxide, BPSG, PSG, and are used to form the layers which abut the via.